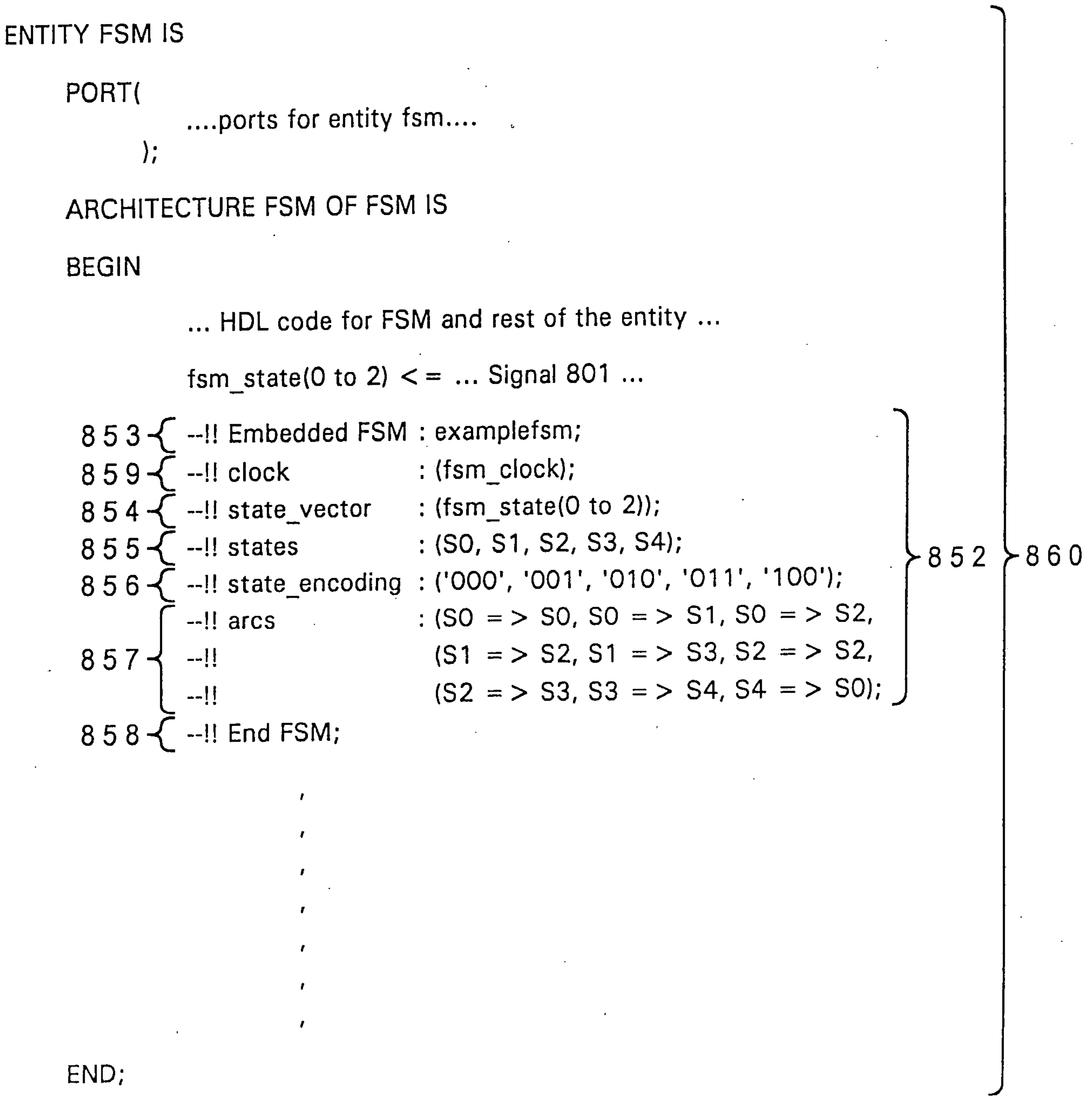


```
ENTITY FSM IS

     PORT(
               ....ports for entity fsm....
          );

     ARCHITECTURE FSM OF FSM IS

     BEGIN

               ... HDL code for FSM and rest of the entity ...

               fsm_state(0 to 2) < = ... Signal 801 ...

               --!! Embedded FSM   : examplefsm;
               --!! clock          : (fsm_clock);
               --!! state_vector   : (fsm_state(0 to 2));
               --!! states         : (S0, S1, S2, S3, S4);
               --!! state_encoding : ('000', '001', '010', '011', '100');
               --!! arcs           : (S0 = > S0, S0 = > S1, S0 = > S2,
               --!!                   (S1 = > S2, S1 = > S3, S2 = > S2,
               --!!                   (S2 = > S3, S3 = > S4, S4 = > S0);
               --!! End FSM;

                         ,
                         ,
                         ,
                         ,
                         ,
                         ,
                         ,

     END;
```

Fig. 8C
Prior Art

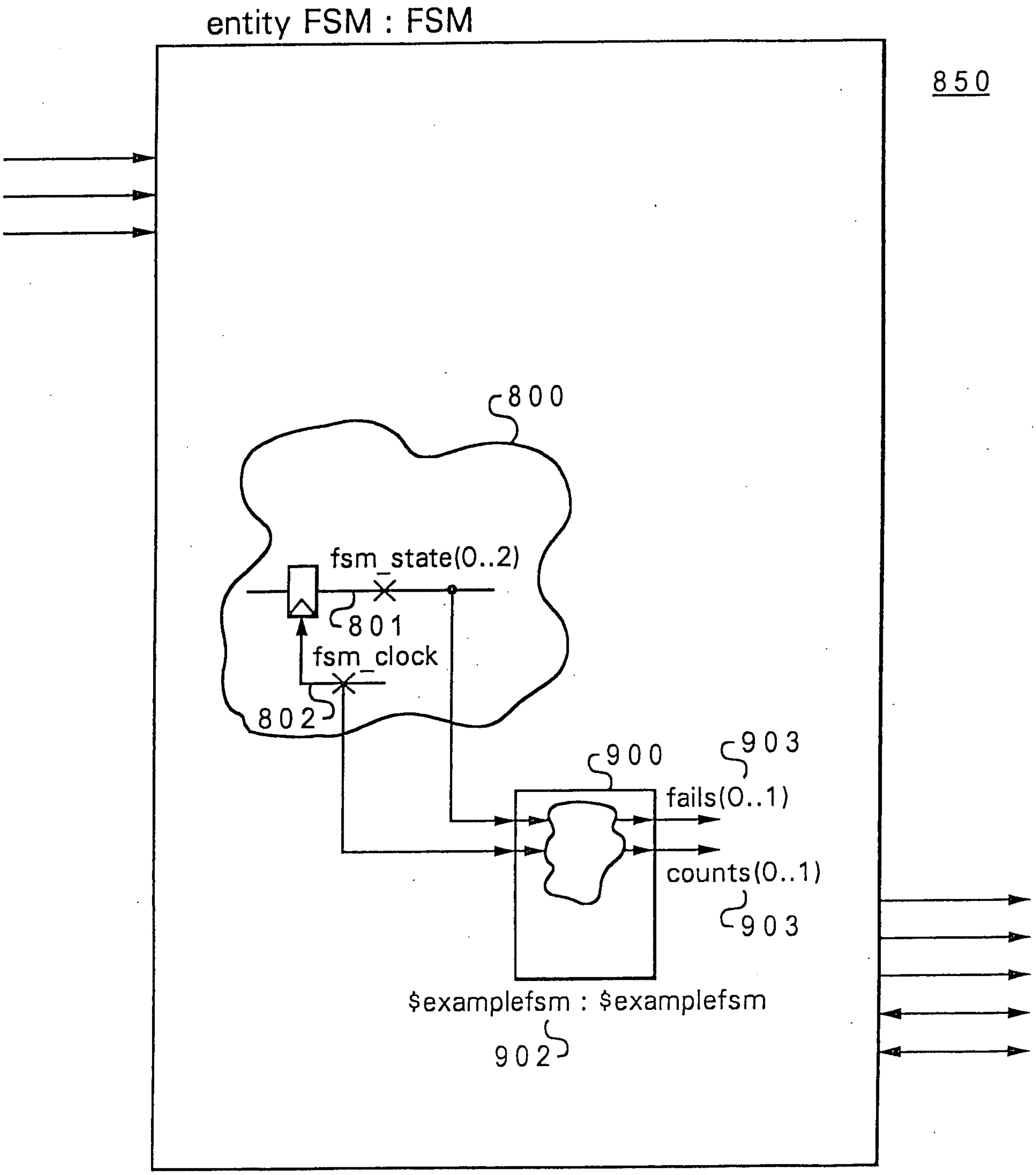
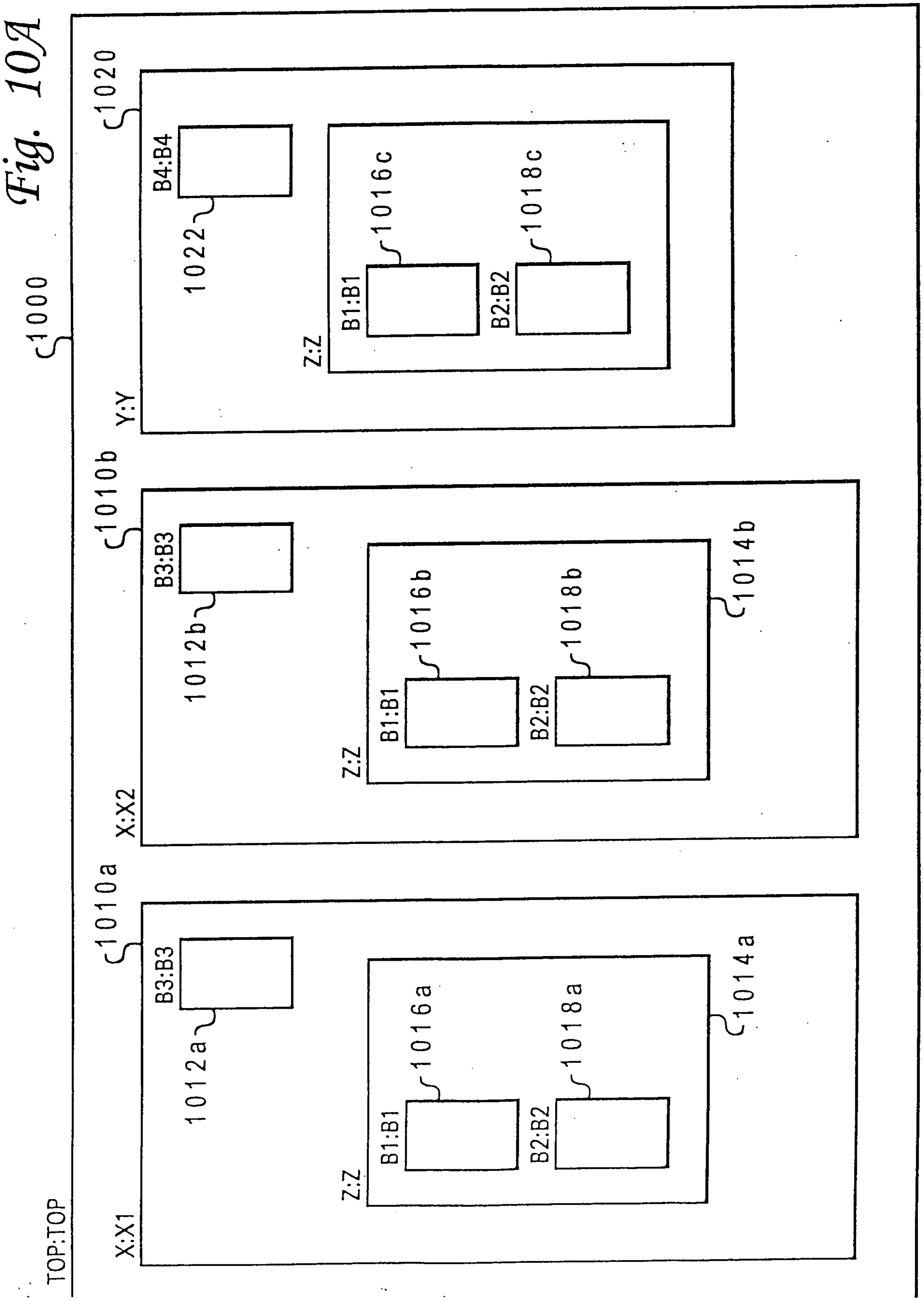
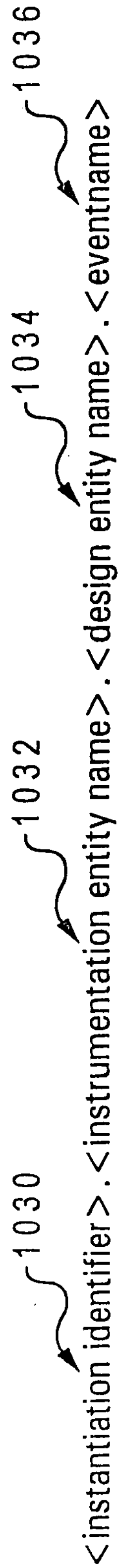


Fig. 9
Prior Art

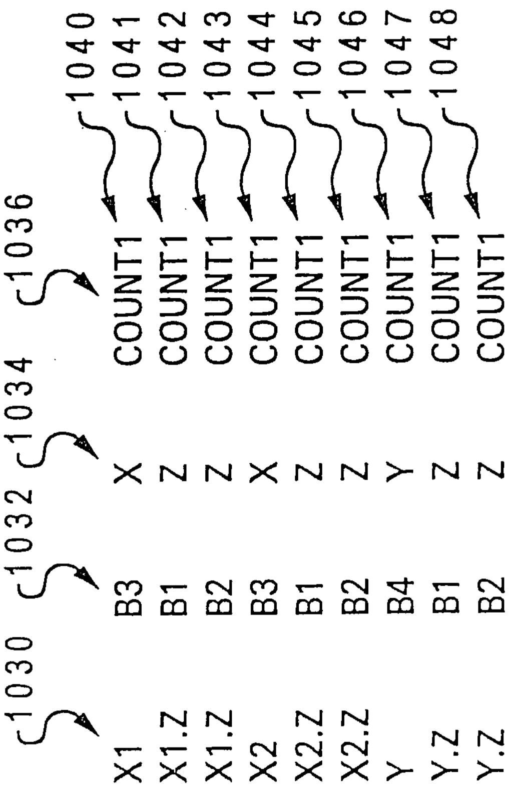
Fig. 10A Prior Art





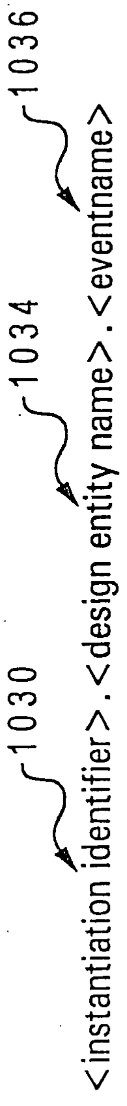
<instantiation identifier>.<instrumentation entity name>.<design entity name>.<eventname>

Fig. 10B


1030
1032
1034
1036
1040
1041
1042
1043
1044
1045
1046
1047
1048

X1	B3	X	COUNT1
X1.Z	B1	Z	COUNT1
X1.Z	B2	Z	COUNT1
X2	B3	X	COUNT1
X2.Z	B1	Z	COUNT1
X2.Z	B2	Z	COUNT1
Y	B4	Y	COUNT1
Y.Z	B1	Z	COUNT1
Y.Z	B2	Z	COUNT1

Fig. 10C



<instantiation identifier>.<design entity name>.<eventname>

Fig. 10D
Prior Art

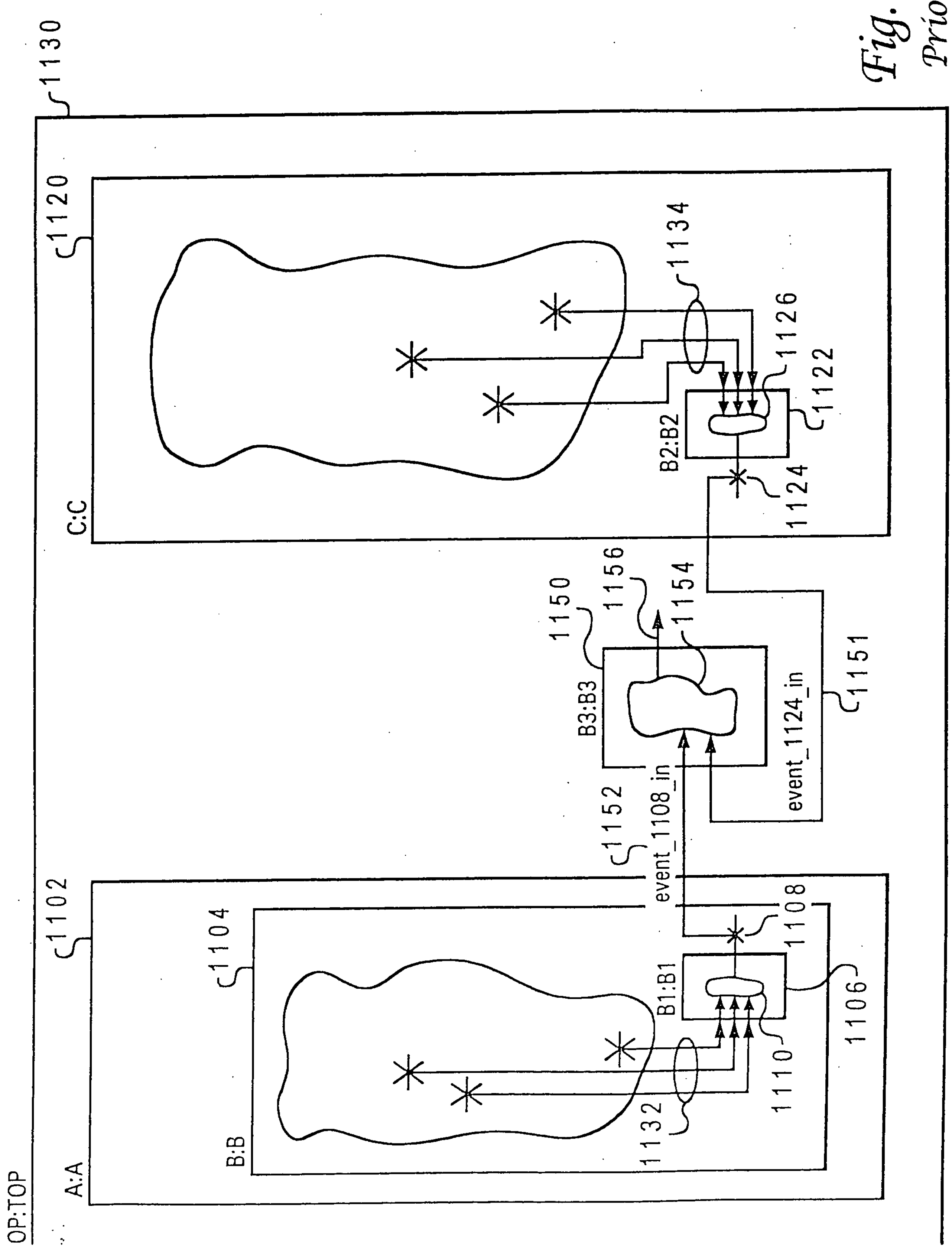
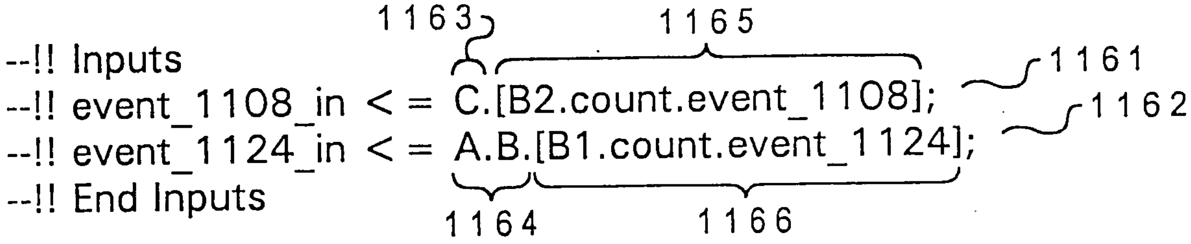
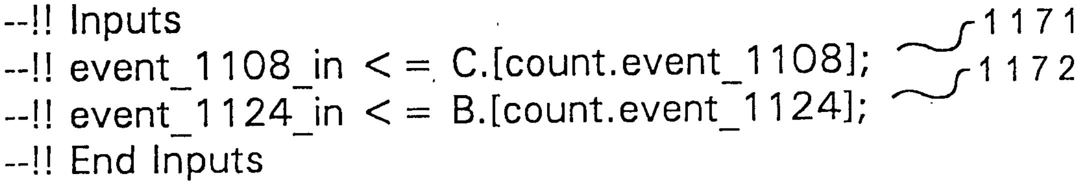


Fig. 11A
Prior Art



```
--!! Inputs
--!! event_1108_in <= C.[B2.count.event_1108];
--!! event_1124_in <= A.B.[B1.count.event_1124];
--!! End Inputs
```

Fig. 11B



```
--!! Inputs
--!! event_1108_in <= C.[count.event_1108];
--!! event_1124_in <= B.[count.event_1124];
--!! End Inputs
```

Fig. 11C

Prior Art

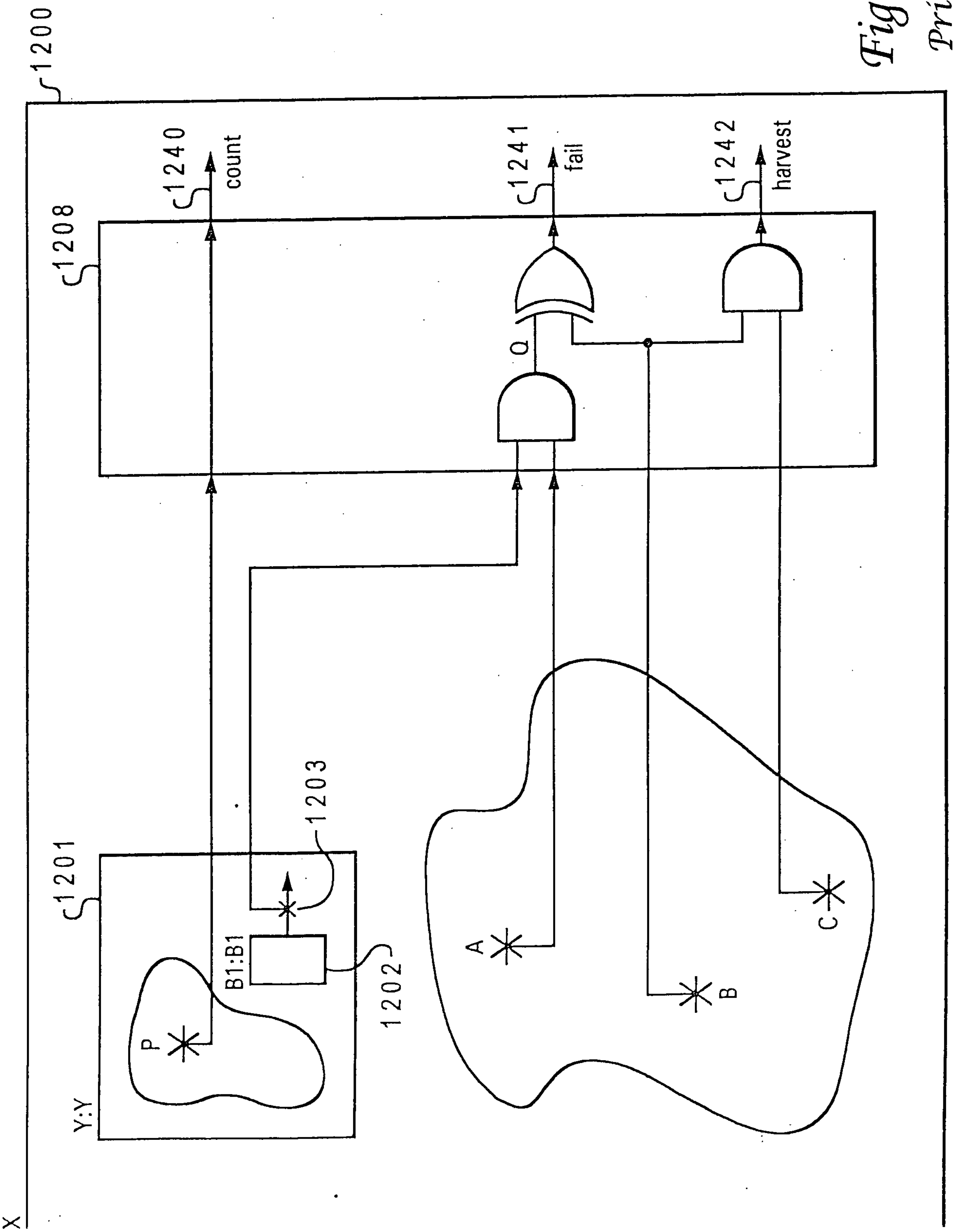
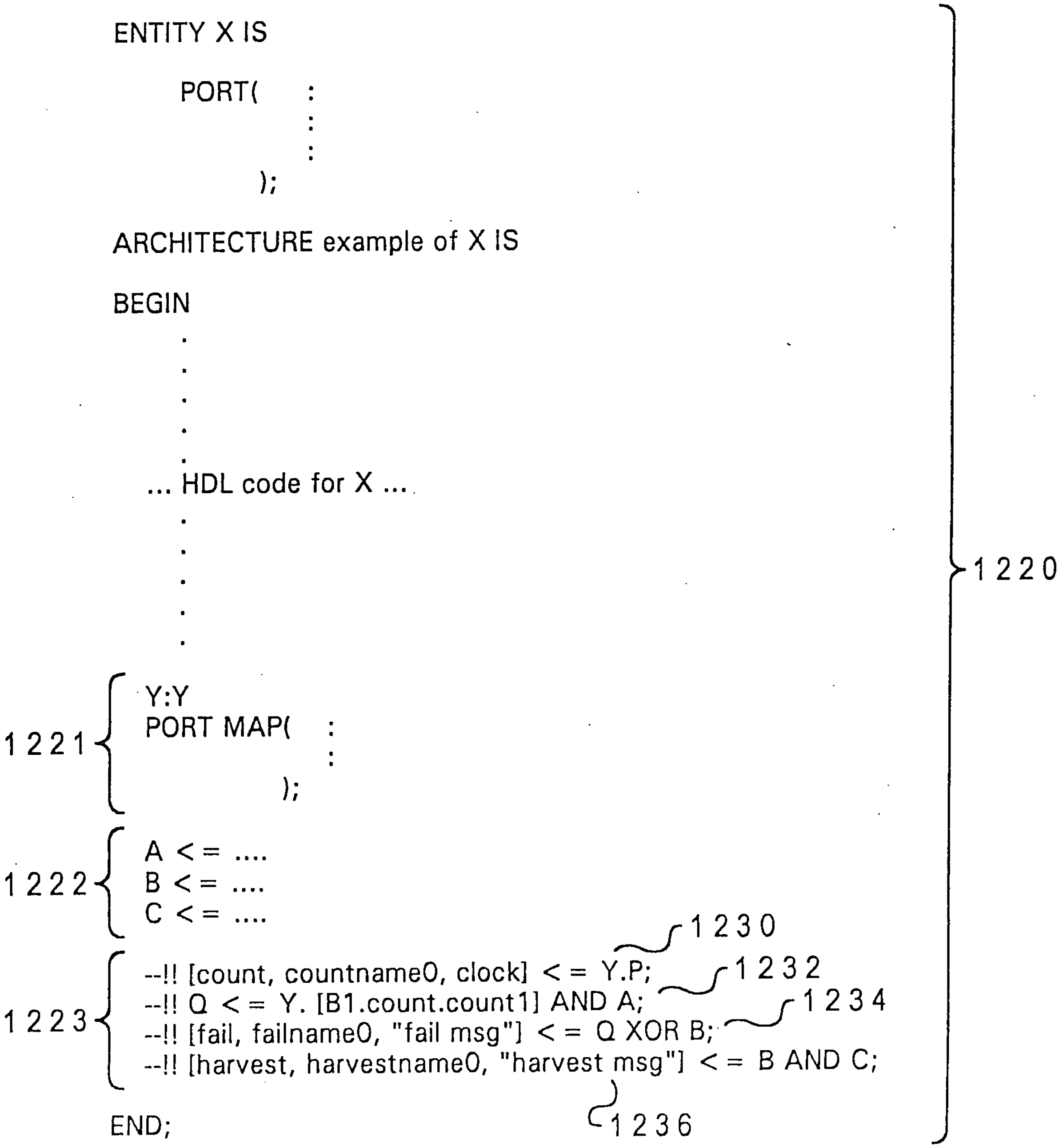


Fig. 12A
Prior Art



```
ENTITY X IS

      PORT(      :
                 :
                 :
                 :
             );

ARCHITECTURE example of X IS

BEGIN
      .
      .
      .
      .
      .
   ... HDL code for X ...
      .
      .
      .
      .
      .

   Y:Y
   PORT MAP(     :
                 :
            );

   A <= ....
   B <= ....
   C <= ....

   --!! [count, countname0, clock] <= Y.P;
   --!! Q <= Y. [B1.count.count1] AND A;
   --!! [fail, failname0, "fail msg"] <= Q XOR B;
   --!! [harvest, harvestname0, "harvest msg"] <= B AND C;

END;
```

Fig. 12B
Prior Art

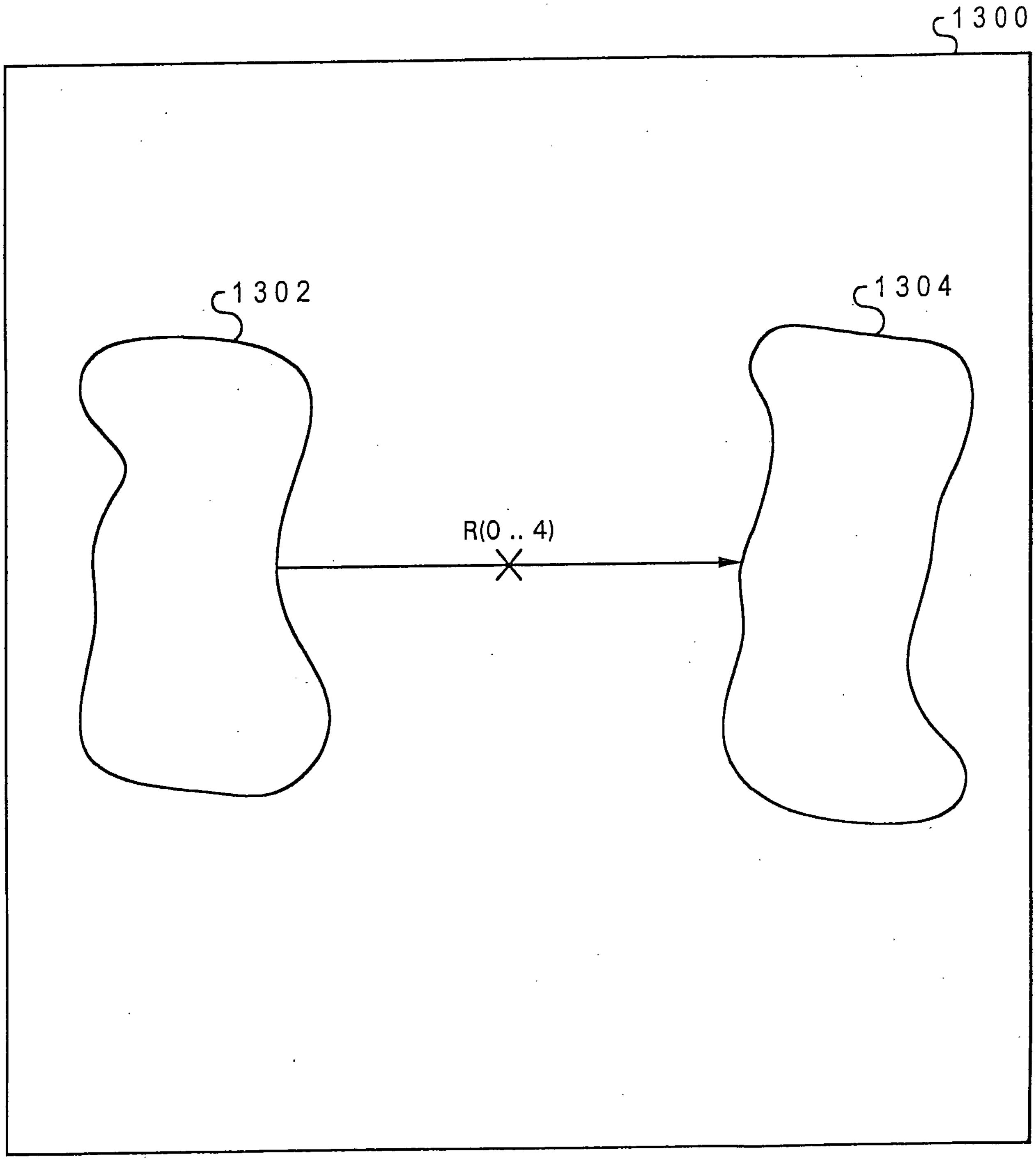


Fig. 13A
Prior Art

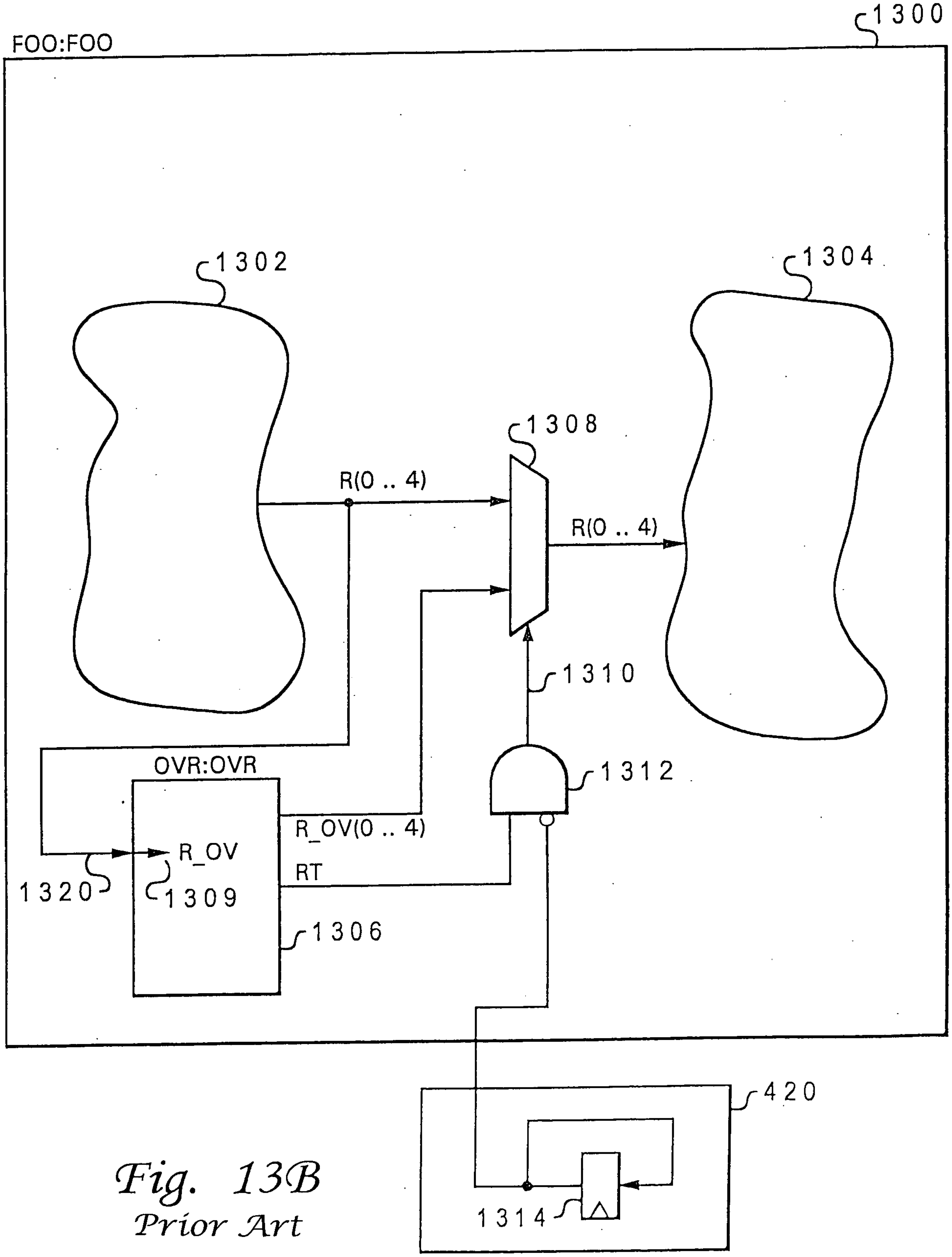
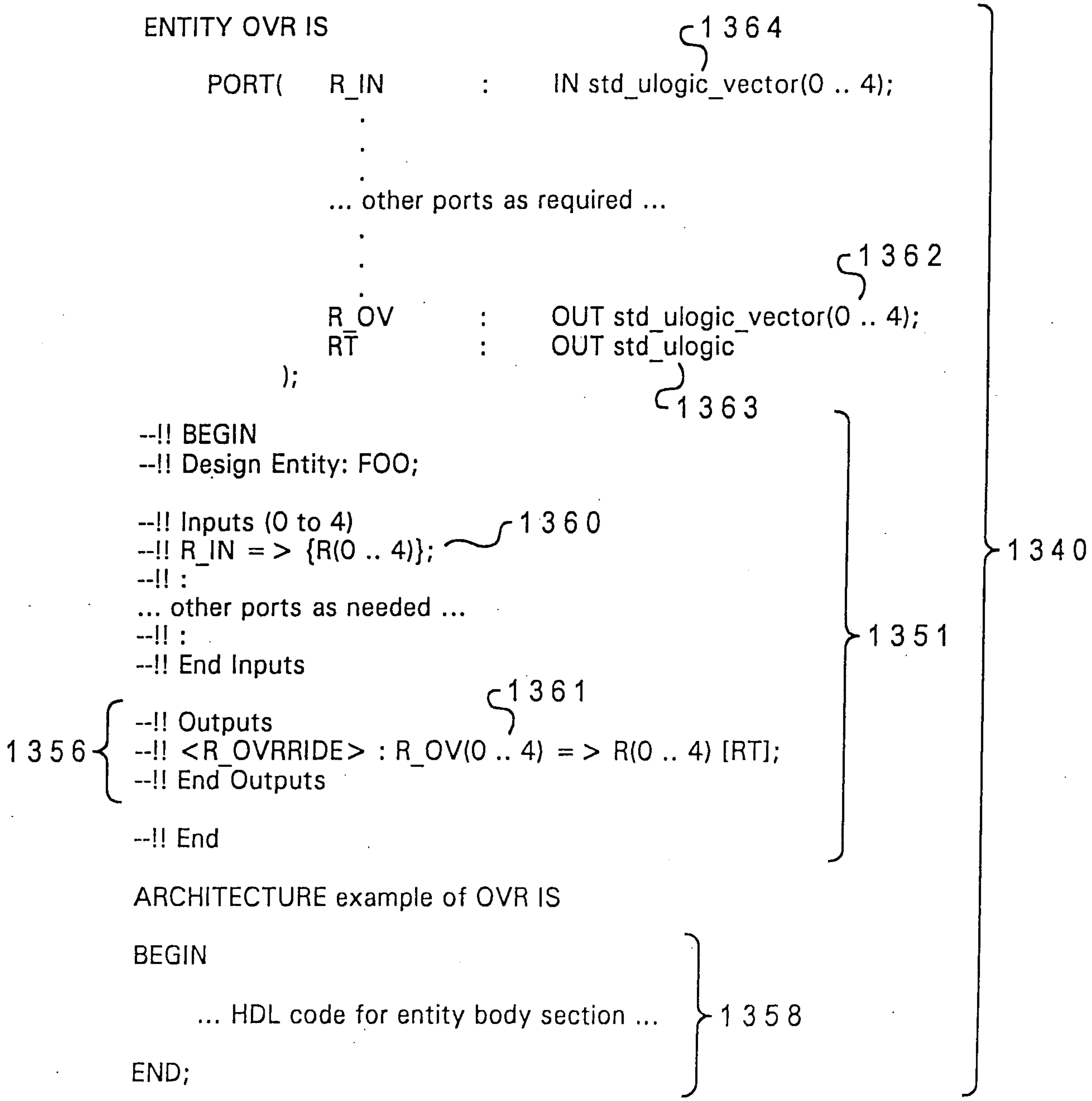
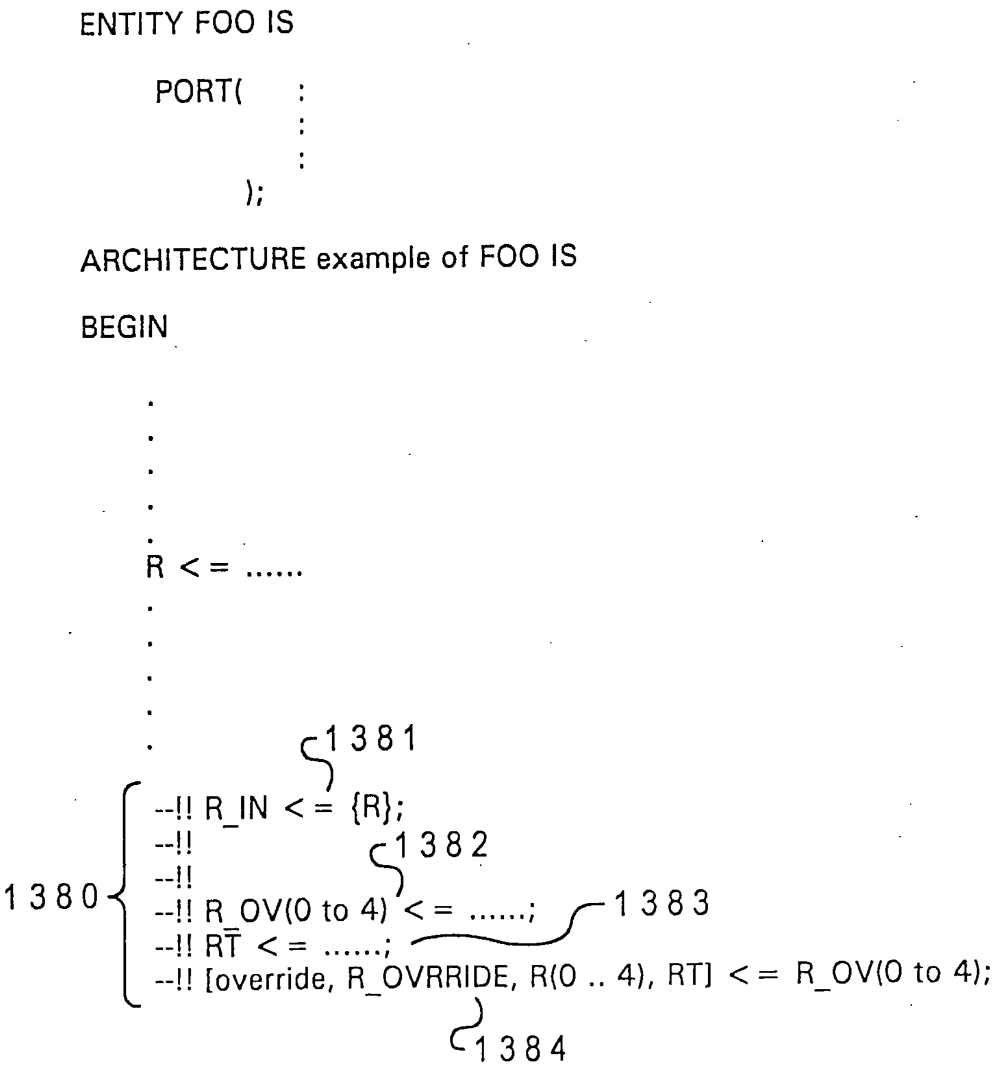


Fig. 13B
Prior Art



```
ENTITY OVR IS

     PORT(    R_IN          :      IN std_ulogic_vector(0 .. 4);
                .
                .
                .
              ... other ports as required ...
                .
                .
                .
              R_OV          :      OUT std_ulogic_vector(0 .. 4);
              RT            :      OUT std_ulogic
          );

--!! BEGIN
--!! Design Entity: FOO;

--!! Inputs (0 to 4)
--!! R_IN => {R(0 .. 4)};
--!! :
... other ports as needed ...
--!! :
--!! End Inputs

--!! Outputs
--!! <R_OVRRIDE> : R_OV(0 .. 4) => R(0 .. 4) [RT];
--!! End Outputs

--!! End

ARCHITECTURE example of OVR IS

BEGIN

     ... HDL code for entity body section ...

END;
```

Fig. 13C
Prior Art



```
ENTITY FOO IS

      PORT(     :
                :
                :
                :
            );

ARCHITECTURE example of FOO IS

BEGIN

      .
      .
      .
      .
      .
      R <= ......
      .
      .
      .
      .
      .

      --!! R_IN <= {R};
      --!!
      --!!
      --!! R_OV(0 to 4) <= ......;
      --!! RT̄ <= ......;
      --!! [override, R_OVRRIDE, R(0 .. 4), RT] <= R_OV(0 to 4);
```

Fig. 13D

Prior Art

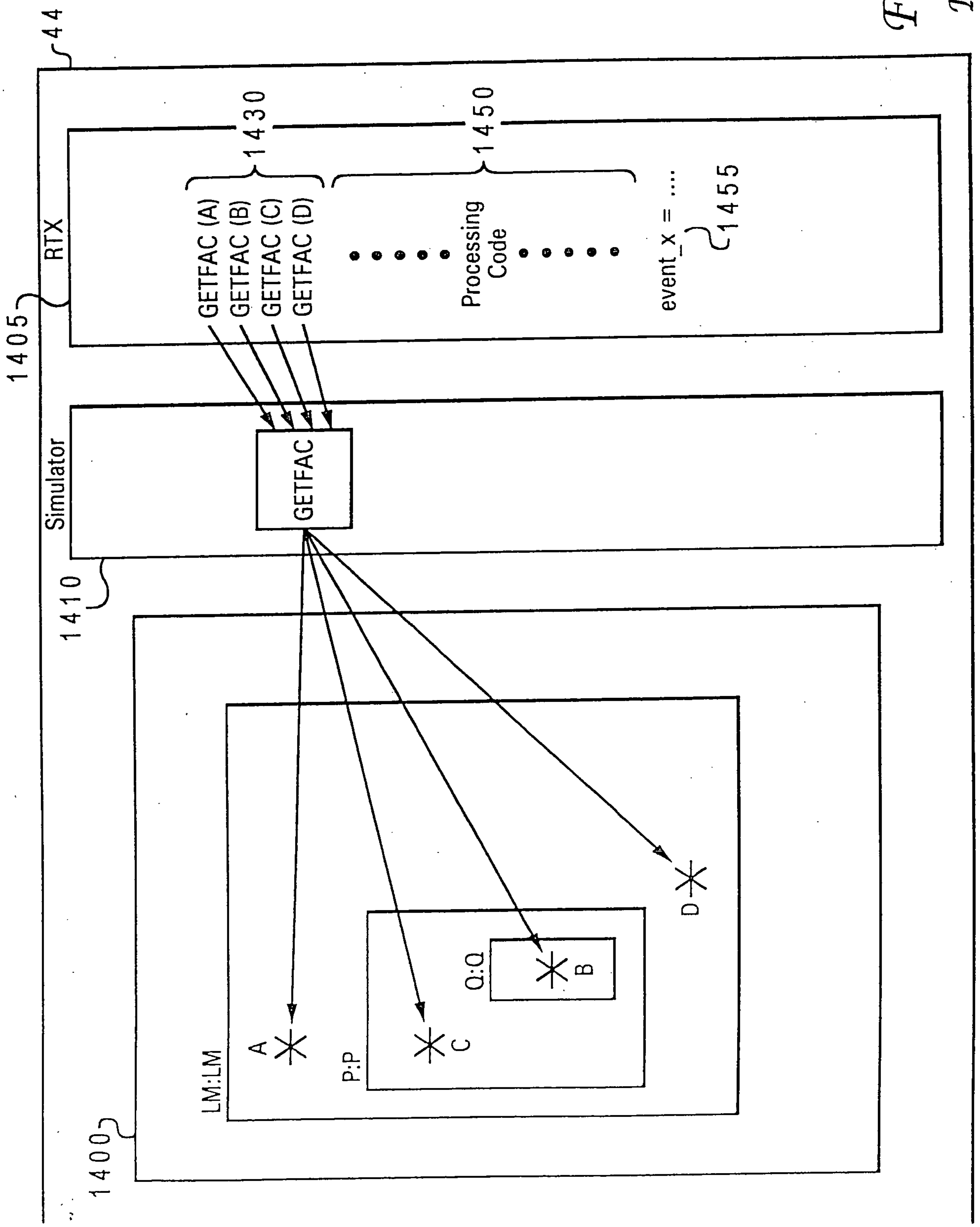


Fig. 14A
Prior Art

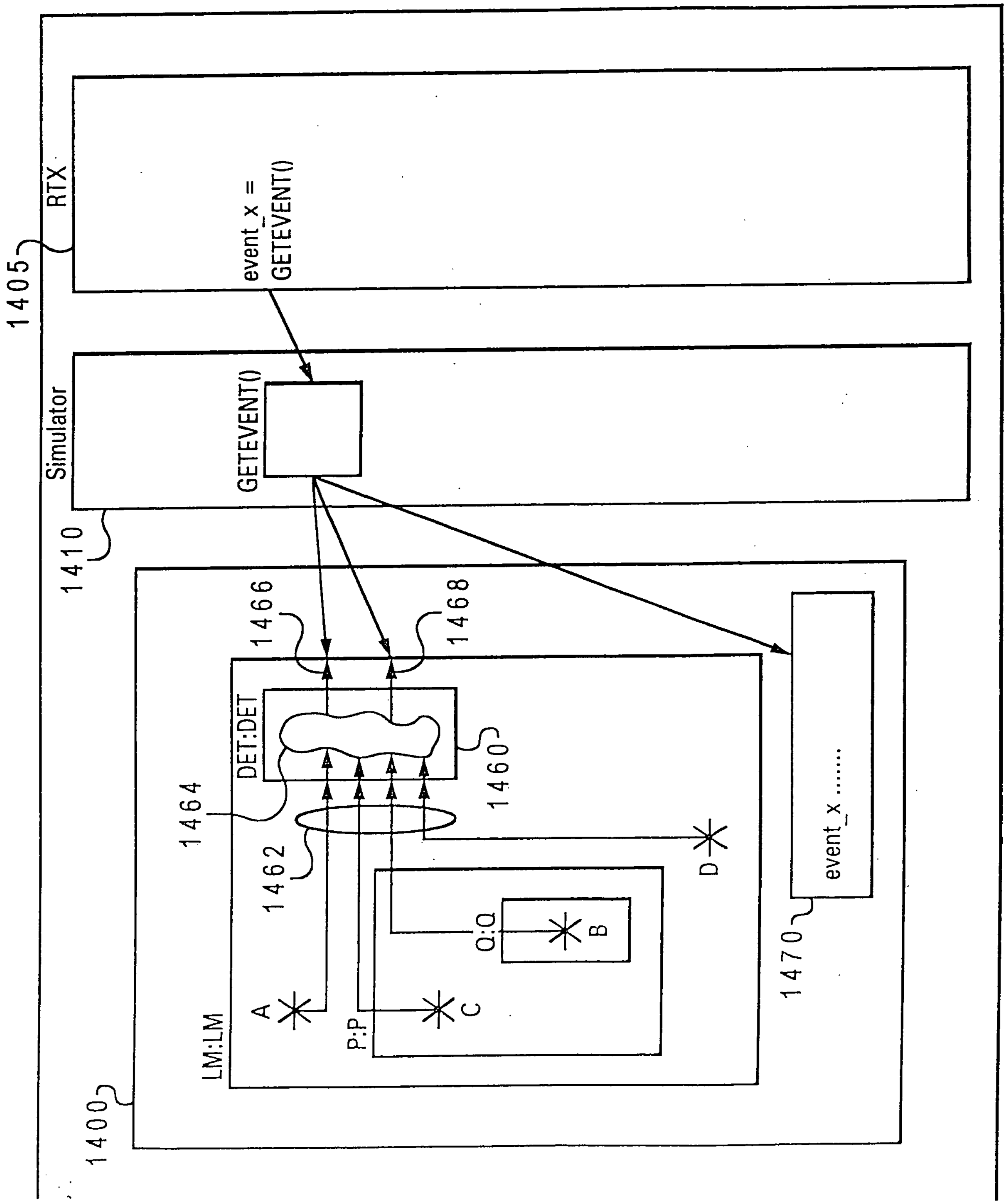
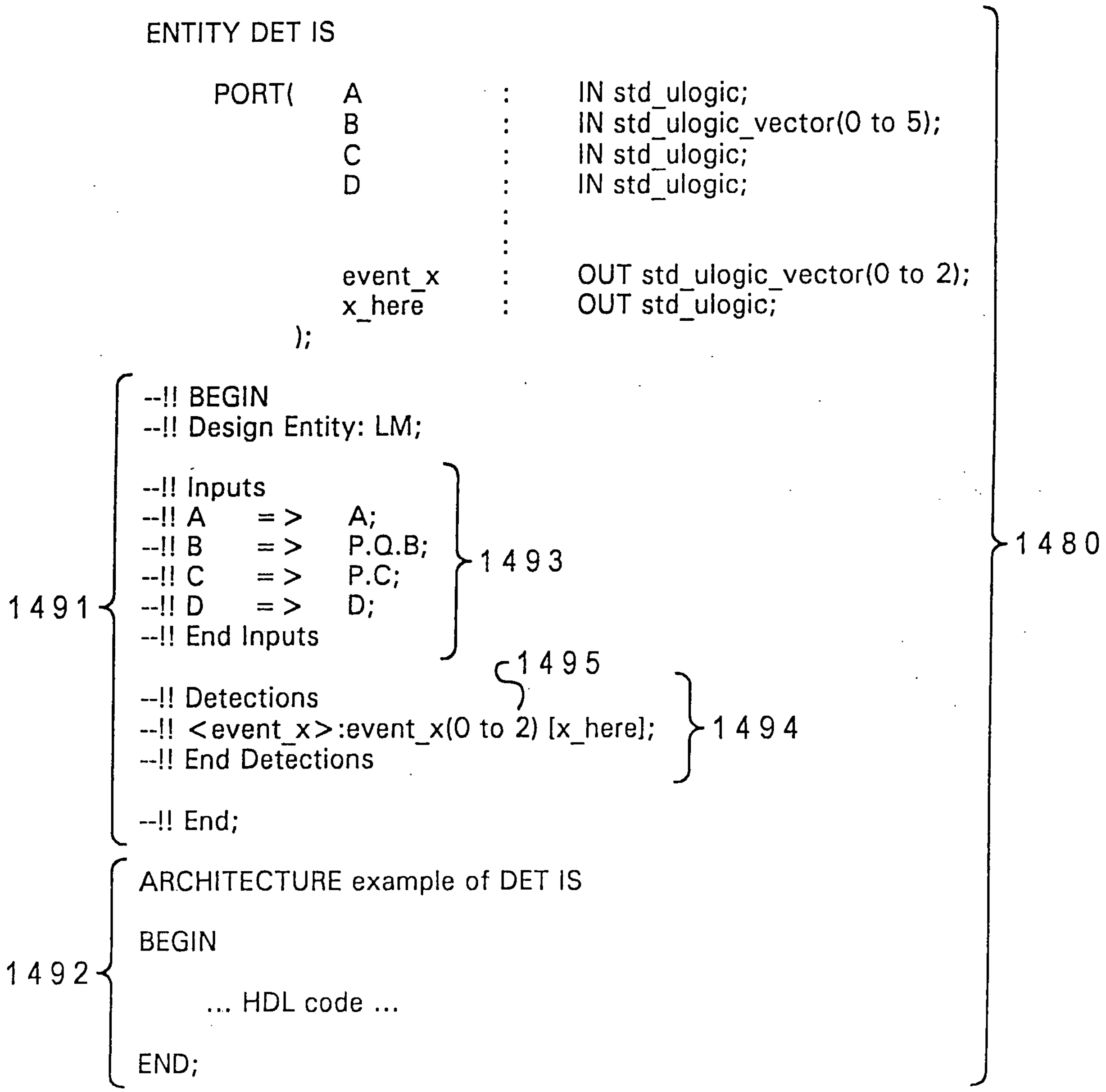


Fig. 14B
Prior Art



```
ENTITY DET IS

      PORT(   A            :      IN std_ulogic;
              B            :      IN std_ulogic_vector(0 to 5);
              C            :      IN std_ulogic;
              D            :      IN std_ulogic;
                           :
                           :
              event_x      :      OUT std_ulogic_vector(0 to 2);
              x_here       :      OUT std_ulogic;
           );

--!! BEGIN
--!! Design Entity: LM;

--!! Inputs
--!! A      =>     A;
--!! B      =>     P.Q.B;
--!! C      =>     P.C;
--!! D      =>     D;
--!! End Inputs

--!! Detections
--!! <event_x>:event_x(0 to 2) [x_here];
--!! End Detections

--!! End;

ARCHITECTURE example of DET IS

BEGIN

      ... HDL code ...

END;
```

Fig. 14C

Prior Art